2633
B194

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Jun Cao
Application No.	:	09/784,419
Filed	:	February 15, 2001
Title	:	LINEAR FULL RATE PHASE DETECTOR AND CLOCK DATA RECOVERY CIRCUIT
Grp./Div.	:	2633
Examiner	:	David C. Payne
Docket No.	:	50987/RJP/B600

STATUS INQUIRY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 7068
Pasadena, CA 91109-7068
August 30, 2004

Commissioner:

This is to inquire as to the status of the Substitution of Attorney with Change of Address for Correspondence by Assignee filed on September 29, 2003, a copy of which is enclosed. Applicant respectfully requests confirmation of this submission.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
Colin Dorrian
Reg. No. 54,658
626/795-9900

CTD/srh
Enclosure

SH PAS581374.1-*-08/25/04 9:37 AM

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on: 8/31/04
(Date of Deposit)

50987-DBP-B600

PATENT

ART UNIT 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 30/DBP/B600

SUBSTITUTION OF ATTORNEY WITH
CHANGE OF ADDRESS FOR CORRESPONDENCE
BY ASSIGNEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Broadcom Corporation, assignee of the entire interest in and to each U.S. patent application, identified on Exhibit A attached, under an Assignment recorded in the U.S. Patent and Trademark Office, hereby revokes all previous Powers of Attorney and appoints:

D. Bruce Prout	(20,958)	Harold E. Wurst	(22,183)	Jun-Young E. Jeon	(43,693)
Richard J. Ward, Jr.	(24,187)	Robert A. Green	(28,301)	Peter A. Nichols	(47,822)
LeRoy T. Rahn	(20,356)	Richard A. Wallen	(22,671)	Stephen D. Burbach	(40,285)
Walter G. Maxwell	(25,355)	Michael J. MacDermott	(29,946)	Mark J. Marcelli	(36,593)
William P. Christie	(29,371)	Anne Wang	(36,045)	David J. Steele	(47,317)
David A. Dillard	(30,831)	Constantine Marantidis	(39,759)	John W. Peck	(44,284)
Thomas J. Daly	(32,213)	Daniel R. Kimbell	(34,849)	Tom H. Dao	(44,641)
Vincent G. Gioia	(19,959)	Daniel M. Cavanagh	(41,661)	Frank L. Cire	(42,419)
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John D. Carpenter	(34,133)	Kathleen M. Olster	(42,052)	R. W. Johnston	(17,968)
Wesley W. Monroe	(39,778)	Josephine E. Chang	(46,083)	Hayden A. Carney	(22,653)
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Gregory S. Lampert	(35,581)	Patrick Y. Ikehara	(42,681)	Richard D. Seibel	(22,134)
Mark Garscia	(31,953)	Raymond R. Tabandeh	(43,945)	Richard J. Paciulan	(28,248)
Syed A. Hasan	(41,057)	Cynthia A. Bonner	(44,548)	Richard A. Clegg	(33,485)

all members or associates of or of counsel to the firm CHRISTIE, PARKER & HALE, LLP, telephone (626) 795-9900, as principal attorneys with power to appoint associate attorneys, to prosecute this application and any subsequent application based on the disclosure of this application, and to transact all business in the Patent and Trademark Office connected with this application and any subsequent application.

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9/29/03
(Date of Deposit)

The authority under this Power of Attorney of each person named above shall automatically terminate and be revoked upon such person ceasing to be a member or associate of or of counsel to that law firm.

Please address all correspondence to **CHRISTIE, PARKER & HALE, LLP, P.O. Box 7068, Pasadena, California 91109-7068. Customer Number: 23363**

Broadcom Corporation

Date: September 12, 2003

By _____
Print Name: Dee Henderson
Title: Intellectual Property Portfolio Manager

DBP/djp

DJP PAS524724.1-*-09/5/03 9:47 AM

CPH/BP No.	Application No.	Filing Date	Title
/BP1646	09/614,308	7/12/2000	Fast Acquisition Phase Locked Loop Using a Current DAC
50944/BP1647	09/540,243/ 6,526,113	3/31/2000/ 2/25/03	GM Cell Based Control Loops
/BP1648	09/632,665	8/7/2000	CMOS Lock Detect With Double Protection
50955/BP1649	09/632,666	8/7/2000	Built-In Shelf Test for Multi-Channel Transceivers without Data Alignment
/BP1651	09/615,033/ 6,389,092	7/12/2000/ 5/14/2002	Stable Phase Locked Loop Having Separated Pole
/BP1651CON	10/095,556/ 6,549,599	3/11/2002/ 4/15/2003	Stable Phase Locked Loop Having Separated Pole
50952/BP1653	09/792,684/ 6,566,971	2/24/01/ 5/20/2003	Method and Circuitry for Implementing a Differentially Tuned Varactor-Inductor Oscillator
50953/BP1653CON	10/407,909	4/2/2003	Method and Circuitry for Implementing a Differentially Tuned Varactor-Inductor Oscillator
/BP1654	09/782,687	2/12/2001	Linear Half-Rate Phase Detector and Clock and Data Recovery Circuit
/BP1655	09/784,419	2/15/2001	Linear Full-Rate Phase Detector and Clock and Data Recovery Circuit
50947/BP1656	09/772,781/ 6,396,894	1/29/2001/ 5/28/2002	Overflow Detector for FIFO
50948/BP1656CON1	10/104,870/ 6,519,311	3/21/2002/ 2/11/2003	Overflow Detector for FIFO
/BP1657	09/788,220/ 6,396,360	2/16/2001/ 5/28/2002	Method and Circuitry for Implementing an Inductor-Capacitor Phase Interpolated Voltage-Controlled Oscillator
/BP1658	09/650,275	8/29/2000	Seal Ring for Integrated Circuits
/BP1660	09/919,636	7/31/2001	Fully Differential CMOS Phase-Locked Loop
/BP1815	09/860,284	5/18/2001	Varactor Based Differential VO Band Switching
50957/BP1818	10/037,897	10/22/2001	Methods and Circuitry for Reducing Intermodulation in Integrated Transceivers

CPH/BP No.	Application No.	Filing Date	Title
/BP1851	09/927,705	8/10/2001	Line Loop Back for Very High Speed Application
50950/BP1883DIV	10/267,054	10/7/2002	Low Voltage Differential to Single-Ended Converter
/BP1885	09/910,436	7/19/2001	Synchronous Data Serialization Circuit
/BP1885CON	10/431,103	5/6/2003	Synchronous Data Serialization Circuit
50958/BP1884	09/955,693	9/18/2001	Linear Phase Detector for High Speed Clock data Recovery
50945/BP2015	09/969,837	10/1/2001	High-Speed Peak Amplitude Comparator
/BP2137	10/159,788	5/30/2002	Method and Apparatus for High Speed Signal Recovery
50956/BP2138	10/092,166	3/4/2002	High Frequency Statistical Loss of Signal Detector
50964/BP2144	10/241,140	9/10/2002	Phase Lock Loop with Cycle Drop and Add Circuitry
50963/BP2233	10/243,086	9/12/2002	Delay Generator
50959/BP2233.1	10/243,281	9/12/2002	Symmetric Differential Logic Circuits
50960/BP2360	10/293,163	11/12/2002	Phase Detector for Extended Linear Response and High-Speed Data Regeneration
50961/BP2361	10/293,624	11/12/2002	Phase Detector with Delay Elements for Optimum Data Regneration
50962/BP2385	10/335,190	12/30/2002	CDR Lock Detector with Hysteresis
50896/BP2454	09/747,392	12/22/2000	Methods of Recording Voice Signals in a Mobile Set
/BP2445	09/640,963	8/16/2000	Code Puncturing Method and Apparatus
/BP2446	09/636,000	8/9/2000	Maximum Likelihood Sequence Estimator which Computes Branch Metrics in Real Time
/BP2448	10/228,165	8/26/2002	Frequency Offset Correction Circuit for WCDMA
/BP2449	10/242,319	9/11/2002	MPSK Equalizer
/BP2450	10/272,507	10/15/2002	Shifted 8PSK Modulator for EDGE

PLEASE SIGN AND RETURN TO ACKNOWLEDGE RECEIPT

Title Linear Full-Rate Phase Detector and Clock...

Ser/~~Pat/Reg~~ No: 09/784,419

Filed/~~Issued~~ : 2-15-01

____ Assigned Enclosed (List Assignee)

Client ID B600

Case No 30987

Atty/Sec DJP/d

Date Mailed 9-29-03

Date Due 10-17-0

Cert of Mailing Yes

Express Mail No.

Checked by:

DOCUMENT TITLE:
(List enclosures)

Sub of Attorney with Change of Address

ACKNOWLEDGE HERE

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